Amendments to the Claims

1. (CURRENTLY AMENDED) An active matrix array device comprising an array of individually addressable matrix elements and driver circuitry ~~(65)~~ for providing address signals to the matrix elements, the driver circuitry ~~(65)~~ including digital to analogue converter circuitry for providing a first number (X) of outputs for application in parallel to a corresponding first number of matrix elements, wherein the driver circuitry is arranged alongside one edge of the array of matrix elements, and comprises:

a multiple voltage level generator circuit ~~(16)~~ providing a plurality of analogue voltage levels ($V_0 - V_{M-1}$) for addressing the matrix elements, the plurality of levels being provided on outputs ~~(28)~~ distributed substantially along the length of the one edge;

a group of switches ~~(30)~~ associated with, and located at, each output ~~(28)~~ of the voltage level generator circuit ~~(16)~~; and

an output bus ~~(32)~~ arranged alongside the one edge and having the first number (X) of lines, the group of switches ~~(30)~~ selectively coupling the associated voltage level generator circuit output to each line of the output bus ~~(32)~~.

2. (CURRENTLY AMENDED) A device as claimed in claim 1, wherein the multiple voltage level generator circuit ~~(16)~~ comprises a resistor string extending alongside the length of the one edge.

3. (CURRENTLY AMENDED) A device as claimed in ~~claim 1 or 2~~claim 1, wherein each group (30) of switches comprises a switch associated with each output bus line.

4. (CURRENTLY AMENDED) A device as claimed in claim 3, wherein the switches of each group are controlled by a corresponding bit ~~(S)~~ of digital words based on the digital inputs to the digital to analogue converter circuitry.

5. (ORIGINAL) A device as claimed in claim 4, wherein the digital words comprise the expansion of n-bit digital inputs to the digital to analogue converter

circuitry into 2^n bit words having a single non-zero bit.

6. (CURRENTLY AMENDED) A device as claimed in any preceding claim further comprising a multiplexer circuit ~~(2)~~ for switching the first number (X) of outputs to a selected first number of matrix elements.

7. (CURRENTLY AMENDED) A device as claimed in claim 6, wherein the array of matrix elements are arranged in rows ~~(54)~~ and columns ~~(56)~~, and the driver circuitry ~~(65)~~ is arranged alongside a column edge of the array, and wherein the multiplexer circuit ~~(2)~~ switches the first number of outputs to a selected subset of the columns.

8. (ORIGINAL) A device as claimed in claim 7, wherein the multiplexer circuit comprises the output bus and switching elements which connect to the output bus and to each column.

9. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim~~claim 1, further comprising decoder circuitry ~~(42)~~ for converting n-bit digital inputs to the digital to analogue converter circuitry into 2^n bit words having a single non-zero bit.

10. (CURRENTLY AMENDED) A device as claimed in claim 9, wherein the decoder circuitry ~~(42)~~ is distributed along the length of the one edge and receives the first number of n-bit digital inputs (Data1 – DataX), and generates the first number of 2^n bit digital outputs, with corresponding bits of each of the first number of 2^n bit digital outputs spatially grouped together.

11. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim~~claim 1, comprising an active matrix liquid crystal display.

12. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim~~claim 1, wherein the driver circuitry is integrated onto the same substrate ~~(66)~~ as the array of matrix elements.